MOS
LSI

TMS 4045 JL, NL; TMS 4047 JL, NL
1024 WORD BY 4-BIT STATIC RAM

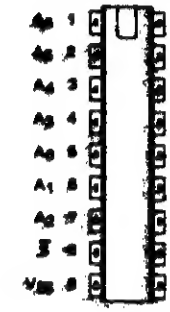
NOVEMBER 1977

- 1024 X 4 Organization
- Single +5 V, ±10% Supply
- High Density 18-and 20-pin Packages
- Fully Static Operation (No clocks, no refresh, no timing strobe)
- 5 Performance Ranges

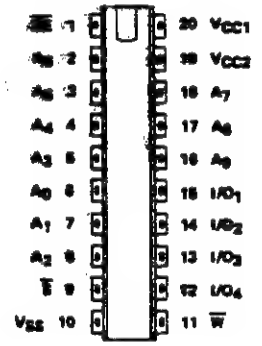
	ACCESS TIME (MAX)	READ OR WRITE CYCLE TIME (MIN)
TMS 4045-15, TMS 4047-15	150 ns	150 ns
TMS 4045-20, TMS 4047-20	200 ns	200 ns
TMS 4045-25, TMS 4047-25	250 ns	250 ns
TMS 4045-30, TMS 4045-30	300 ns	300 ns
TMS 4045-45, TMS 4047-45	450 ns	450 ns

- 400-mV Guaranteed DC Noise Immunity With Standard TTL Loads — No Pull-Up Resistors Required
- Common I/O With Three-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 1 Series 74 or 74S TTL Load — No Pull-Up Resistors Required
- Low Power Dissipation
  - 400 mW (–25, –30, –45) Maximum
  - 550 mW (–15, –20) Maximum

TMS 4045
18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



TMS 4047
20-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 1024 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74 or 74S TTL. No pull-up resistors are required. The TMS 4045/4047 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. Both the TMS 4045 and TMS 4047 are characterized to retain data at V_{CC} = 2.4 V to reduce power dissipation. Furthermore for applications such as battery backup, the TMS 4047 has separate V_{CC} pin for the array and periphery, and data will be retained if power solely to the array is maintained.

PIN NAMES	
A_0-A_9	Addresses
I/O_1-I/O_4	Data input/output
$\overline{OE}$	Output Enable
$\overline{S}$	Chip Select
V_{CC} (TMS 4045)	+5 V Supply
V_{CC1} (TMS 4047)	+5 V Supply (array only)
V_{CC2} (TMS 4047)	+5 V Supply (periphery only)
V_{SS}	Ground
$\overline{W}$	Write Enable

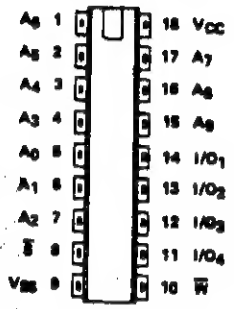
PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

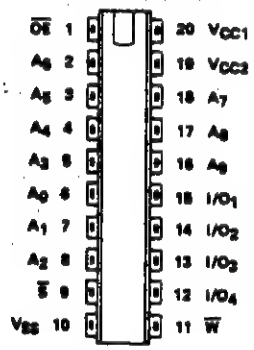
NL; TMS 4047 JL, NL
Y 4-BIT STATIC RAM

NOVEMBER 1977

TMS 4045
18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



TMS 4047
20-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



PIN NAMES	
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I/O_1-I/O_4	Data input/output
$\overline{E}$	Output Enable
	Chip Select
V_{CC} (TMS 4045)	+5 V Supply
V_{CC1} (TMS 4047)	+5 V Supply (array only)
V_{CC2} (TMS 4047)	+5 V Supply (periphery only)
V_{SS}	Ground
	Write Enable

MOS
LSI

TMS4244, TMS4245
4k STATIC RAMs

DECEMBER 1977

- 4096 x 1 and 1024 x 4 Organization
- Plug-compatible with TMS 4044, TMS 4045
- Chip select automatic power down feature
  — Typical standby power 50 mW
- Five performance ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE TIME (MIN)
TMS 4244-15, TMS 4245-15	150 ns	150 ns
TMS 4244-20, TMS 4245-20	200 ns	200 ns
TMS 4244-25, TMS 4245-25	250 ns	250 ns
TMS 4244-30, TMS 4245-30	300 ns	300 ns
TMS 4244-45, TMS 4245-45	450 ns	450 ns

- Single +5-V ± 10% Supply
- Low operating power, 300 mW typical
- High density 18-pin packages
- Fully TTL-compatible with 400-mV guaranteed DC noise immunity with Standard Series 74 TTL.

description

These new 4K fully static random access memories feature automatic chip select power down. They are fully compatible with the existing TMS 4044/4045 series, and allow approximately 80 percent reduction in standby power with no performance degradation. This is achieved by the use of a unique design approach which combines the ease-of-use features associated with non-clocked fully static memories and the reduced standby power dissipation of clocked static memories. Thus the system designer can develop very low power systems without the need for clocks, address set-up and hold times, and reduced data rates caused by cycle times longer than access time.

FUTURE PRODUCTS

117 [illegible] 177

DESIGN GOAL
This document describes the design specifications for a product under development. Texas Instruments reserves the right to change these specifications in any manner, without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5013 • DALLAS, TEXAS 75222

AVAILABLE DURING 1978

SILVERSTAR LTD S.p.A.
Via dei Gracchi, 20

MOTOROLA Semiconductors

MC68488

Advance Information

GENERAL PURPOSE INTERFACE ADAPTER

The MC68488 GPIA provides the means to interface between the IEEE488 standard instrument bus and the MC6800. The 488 instrument bus provides a means for controlling and moving data from complex systems of multiple instruments.

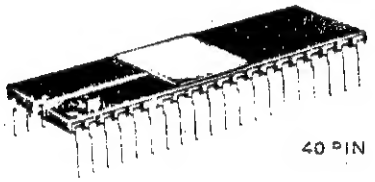
The MC68488 will automatically handle all handshake protocol needed on the instrument bus.

- Single or dual primary address recognition
- Secondary address capability
- Complete source and acceptor handshakes
- Programmable interrupts
- RFD holdoff to prevent data overrun
- Operates with DMA controller
- Serial and parallel polling capability
- Talk-only or listen-only capability
- Selectable automatic features to minimize software
- Synchronization trigger output
- M6800 bus compatible

MOS
(N-CHANNEL, SILICON-GATE DEPLETION LOAD)

GENERAL PURPOSE INTERFACE ADAPTER

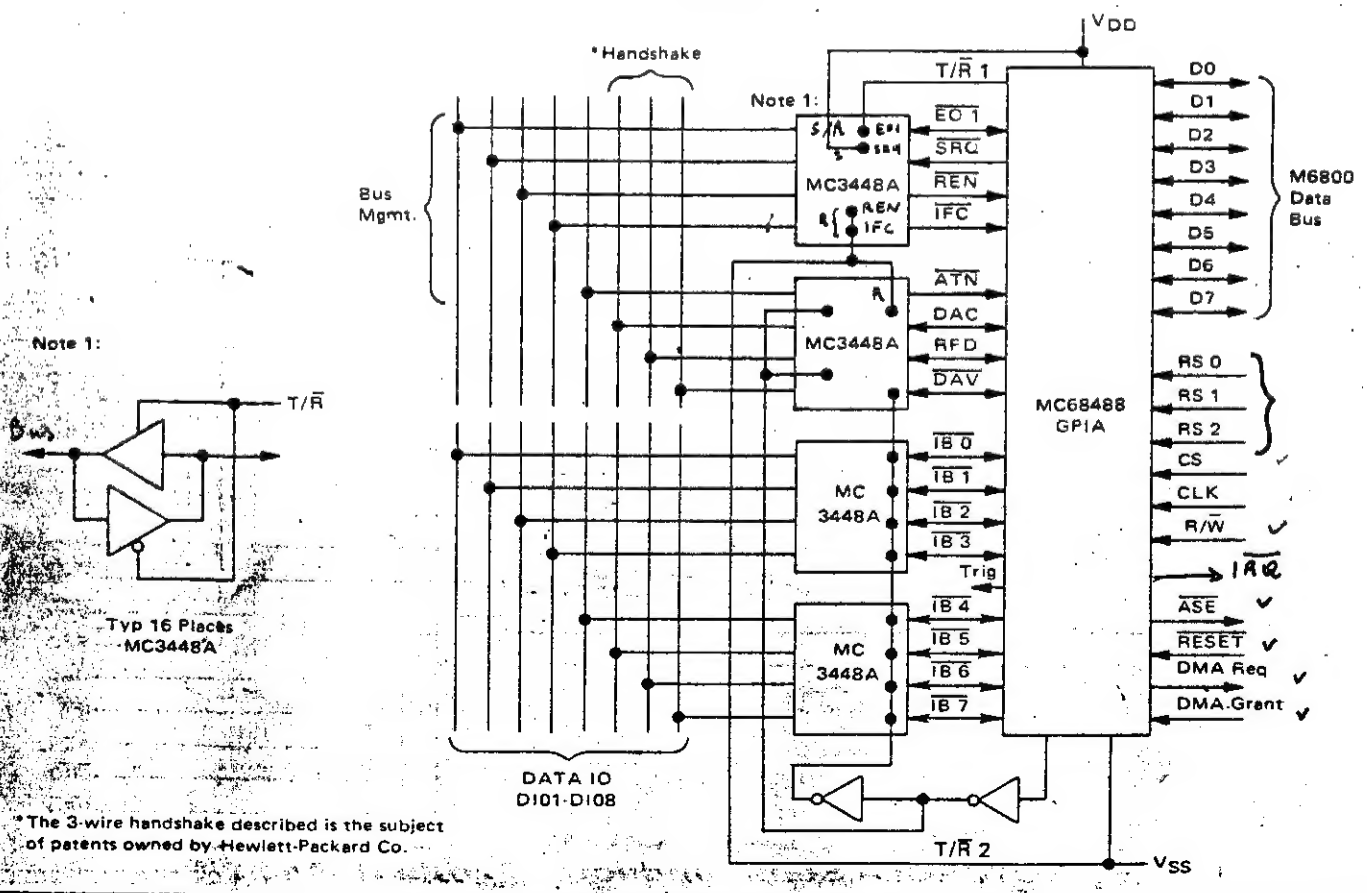
L SUFFIX
CERAMIC PACKAGE
CASE 715



NOT SHOWN:

P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1



*The 3-wire handshake described is the subject of patents owned by Hewlett-Packard Co.

This is advance information and specifications are subject to change without notice

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ADI-462
(Replaces NP-69)

GENERAL DESCRIPTION

The IEEE 488 instrument bus standard is a bit-parallel, byte-serial bus structure designed for communication to and from intelligent instruments. Using this standard, many instruments may be interconnected and remotely and automatically controlled or programmed. Data may be taken from, sent to, or transferred between instruments. A bus controller dictates the role of each device by making the attention line true and sending talk or listen addresses on the instrument bus data lines; those devices which have matching addresses are activated. Device addresses are set into each GPIA from switches or jumpers on a PC board by a microprocessor as a part of the initialization sequence.

When the controller makes the attention line true, instrument bus commands may also be sent to single or multiple GPIA's.

Information is transmitted on the instrument bus data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as the devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices of different speeds to receive the same data concurrently.

The GPIA is designed to work with standard 488-bus driver IC's (MC3448A's) to meet the complete electrical specifications of the IEEE 488 bus. Additionally, a powered-off instrument may be powered-on without disturbing the 488 bus. With some additional logic, the GPIA could be used with other microprocessors.

The MC68488 GPIA has been designed to interface between the MC6800 microprocessor and the complex protocol of the IEEE 488 instrument bus. Many instrument bus protocol functions are handled automatically by the GPIA and require no additional MPU action. Other functions require minimum MPU response due to a large number of internal registers conveying information on the state of the GPIA and the instrument bus.

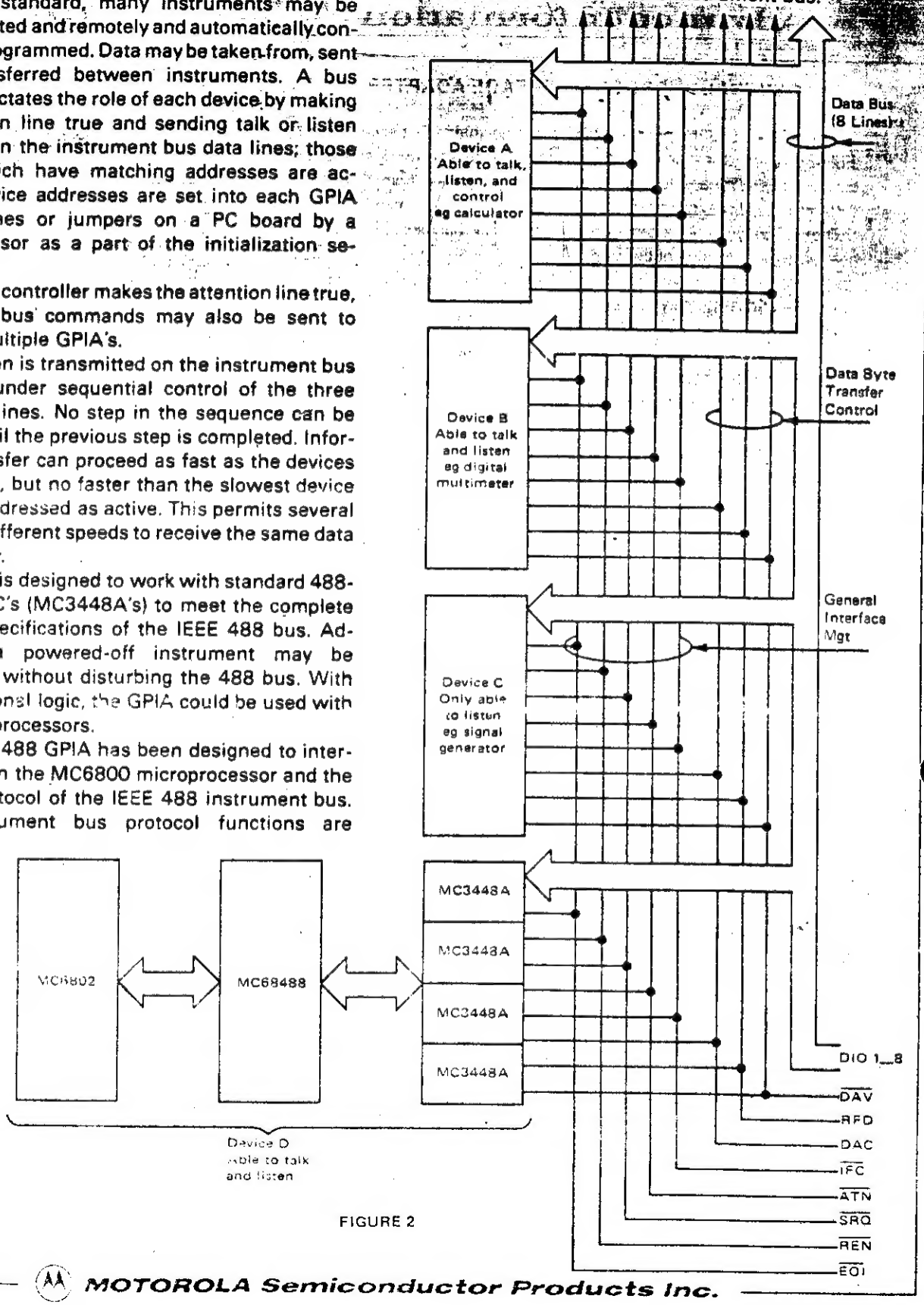


FIGURE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} +2.0	–	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} -0.3	–	V_{SS} +0.8	
Input Leakage Current (V_{in} = 0 to 5.25 V)		I_{in}	-	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V)	D0 - D7	I_{TSI}		2.0	10	μAdc
Output High Voltage (I_{load} = -205 μA)	D0 - D7	V_{OH}	V_{SS} +2.4	–	–	Vdc
Output Low Voltage (I_{load} = 1.6 mA)	D0 - D7	V_{OL}			V_{SS} +0.4	Vdc
(I_{load} = 3.2 mA)	IRQ				V_{SS} +0.4	
Output Leakage Current (Off State) (V_{out} = 0.4 Vdc)	[illegible]	[illegible]		1.0	10	μAdc
[illegible]				600		mW
[illegible] T_A = [illegible]					12.5 7.5	nF

FIGURE 3 - SOURCE and ACCEPTOR HANDSHAKE

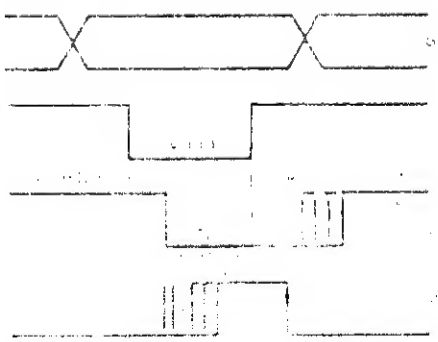
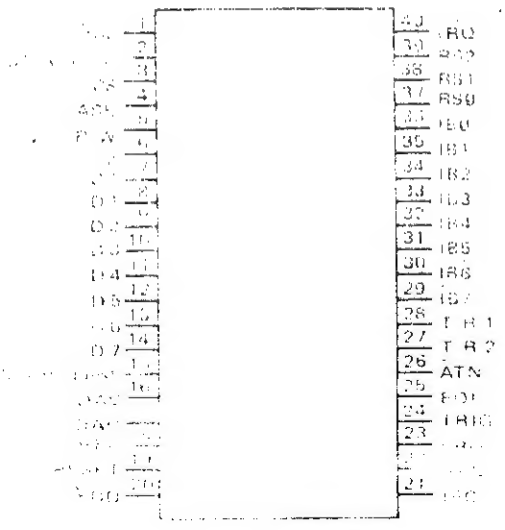


FIGURE 4 - PIN ASSIGNMENT



BUS TIMING CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
READ (See Figure 5)				
Enable Cycle Time	t_{cycE}	1.0	–	µs
Enable Pulse Width, High	PW_{EH}	0.45	–	µs
Enable Pulse Width, Low	PW_{EL}	0.43	–	µs
Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	t_{AS}	160	–	ns
Data Delay Time	t_{DDR}	–	320	ns
Data Hold Time	t_H	10	–	ns
Address Hold Time	t_{AH}	10	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	25	ns
WRITE (See Figure 6)				
Enable Cycle Time	t_{cycE}	1.0	–	µs
Enable Pulse Width, High	PW_{EH}	0.45	–	µs
Enable Pulse Width, Low	PW_{EL}	0.43	–	µs
Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	t_{AS}	160	–	ns
Data Setup Time	t_{DSW}	195	–	ns
Data Hold Time	t_H	10	–	ns
Address Hold Time	t_{AH}	10	–	ns
Rise and Fall Time for Enable input	t_{Er}, T_{Ef}	–	25	ns
OUTPUT (See Figure 7)				
Output Delay Time $\overline{DAV}$, DAC, RFD, $\overline{EOI}$, $\overline{ATN}$ valid T/$\overline{R}$1, T/$\overline{R}$2 valid	 t_{HD} $t_{T/\overline{R}1, 2D}$	 – –	 400 400	 ns ns

FIGURE 5 – BUS READ TIMING CHARACTERISTICS
(Read Information from GPIA)

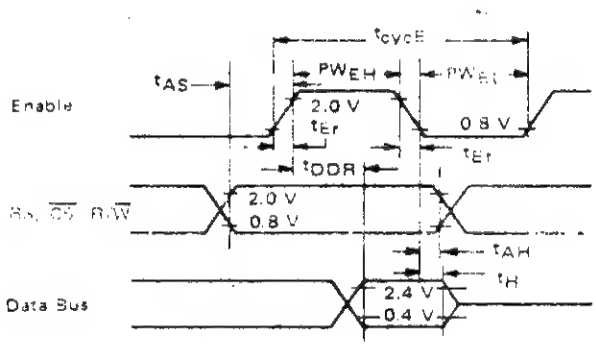


FIGURE 6 – BUS WRITE TIMING CHARACTERISTICS
(Write Information into GPIA)

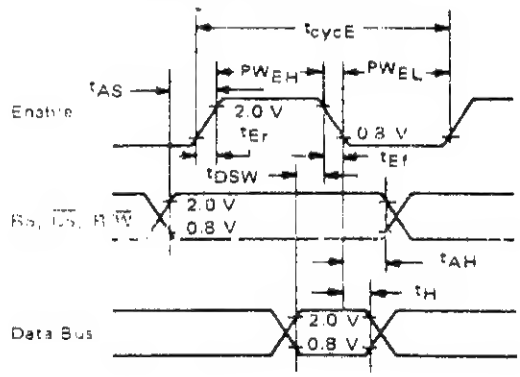
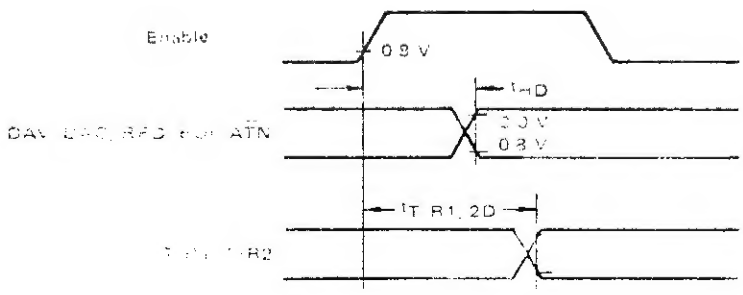


FIGURE 7 – OUTPUT BUS TIMING



AC TIME VALUES

Characteristics		Symbol*	Typ	Unit
Settling Time for Multiple Message	SH	T_1	≥2	μs**
Response to $\overline{ATN}$	SH, AH, T, L	t_2	≤200	ns
Interface Message Accept Time ‡	AH	T_3	>0	§
Response to $\overline{IFC}$ or $\overline{REN}$ False	T, TE, L, LE	t_4	<100	μs
Response to $\overline{ATN}$ • $\overline{EOI}$	PP	t_5	≤200	ns

* Time values specified by a lower case t indicate the maximum time allowed to make a state transition. Time values specified by an upper case T indicate the minimum time that a function must remain in a state before exiting.

**If three-state drivers are used on the $\overline{DIO}$ – $\overline{DAV}$ and $\overline{EOI}$ lines, T_1 may be:
(1) ≥1100 ns
(2) Or ≥700 ns if it is known that within the controller $\overline{ATN}$ is driven by a three-state driver.
(3) Or ≥500 ns for all subsequent bytes following the first sent after each false transition of $\overline{ATN}$ [the first byte must be sent in accordance with (1) or (2)].

‡ Time required for interface functions to accept, not necessarily respond to interface messages.

§ Implementation dependent.

MPU bus clock rate — The current 6800 bus clock is ≤ 1 MHz but part should operate at 1.5 MHz (design goal), with appropriate settling times (T1).

GPIA/MPU INTERFACE SIGNALS

The MC68488 interfaces to the M6800 MPU with an eight-bit bidirectional data bus, a chip select, Read/$\overline{Write}$ line, $\overline{Reset}$ line, three register select lines, an interrupt request line, two DMA control lines, and an address switch enable line.

Bidirectional Data (D0-D7)—The bidirectional data lines allow the transfer of data between the MPU and the GPIA. The data bus output drivers are three state devices that remain in the high impedance (off) state except when the MPU performs a GPIA read operation. The Read/$\overline{Write}$ line is in the read state when the GPIA is selected for a read operation.

Chip Select ($\overline{CS}$)—This input signal is used to select the GPIA. $\overline{CS}$ must be low for selection of the device. Chip select decoding is normally accomplished with logic external to the chip.

Read/$\overline{Write}$ Line (R/$\overline{W}$)—This signal is generated by the MPU to control register access and direction of data transfer on the data bus. A low state on the GPIA Read/$\overline{Write}$ allows for the selection of one of seven write only registers when used in conjunction with the register select lines; RS0, RS1, RS2. A high state on the GPIA Read/$\overline{Write}$ allows for the selection of one of eight read only registers when used in conjunction with register select lines RS0, RS1, RS2.

Register Select (RS0, RS1, RS2)—The three register select lines are used to select the various registers inside the GPIA. These three lines are used in conjunction with the Read/$\overline{Write}$ line to select a particular register that is to be written or read. Table 1 shows the register select coding.

Interrupt Request ($\overline{IRQ}$)—The $\overline{IRQ}$ output goes to the common interrupt bus for the MPU. This is an open drain output which is wire-ORed to the $\overline{IRQ}$ bus. The $\overline{IRQ}$ is set false (low) when an enabled interrupt occurs and stays false until the MPU reads from the interrupt status register.

$\overline{Reset}$—The active low $\overline{Reset}$ line is used to initialize the chip during power on start up. $\overline{Reset}$ will be driven by an external power-up reset circuit.

DMA Control Lines (DMA Grant, DMA Request)—The DMA request line is used to signal waiting data when Byte In (BI) or Byte Out (BO) is set high for a DMA controller. The DMA request line is set high if either the BI or BO interrupt flags are set in the Interrupt Status Register (ROW) and the corresponding bits in the Interrupt Mask Register (ROR) are set true. The DMA request line is cleared when the DMA grant is made true. The DMA grant line is used to signal the GPIA that the DMA controller has control of the MPU data and address lines. **DMA Grant must be grounded when not in use!*

Address Switch Enable ($\overline{ASE}$)—The $\overline{ASE}$ output is used to enable the device address switch three state buffers to allow the instrument address switch to be read on the MPU bus.

Clock Input (Clk)—The Clk input is normally a derivative of the MPU ø2 clock.

TABLE 1 — Register Access

RS2	RS1	RS0	R/W	Register Title	Register Symbol
0	0	0	1	Interrupt Status	R0R
0	0	0	0	Interrupt Mask	R0W
0	0	1	1	Command Status	R1R
0	0	1	0	Unused	—
0	1	0	1	Address Status	R2R
0	1	0	0	Address Mode	R2W
0	1	1	1	Auxiliary Command	R3R
0	1	1	0	Auxiliary Command	R3W
1	0	0	1	Address Switch*	R4R
1	0	0	0	Address	R4W
1	0	1	1	Serial Poll	R5R
1	0	1	0	Serial Poll	R5W
1	1	0	1	Command Pass-Through	R6R
1	1	0	0	Parallel Poll	R6W
1	1	1	1	Data In	R7R
1	1	1	0	Data Out	R7W

*External to MC68488.

GPIA/488 Interface Bus Signals

The GPIA provides a set of eighteen interface signal lines between the M6800 and the IEEE Standard 488 bus.

Signal Lines ($\overline{IB0}$-$\overline{IB7}$)—These bidirectional lines allow for the flow of seven bit ASCII interface messages and device dependent messages. Data appears on these lines in a bit-parallel byte-serial form. These lines are buffered by the MC3448A transceivers and applied to the 488 bus (DIO1-DIO8).

Byte Transfer Lines (DAC, RFD, $\overline{DAV}$)—These lines allow for proper transfer of each data byte on the bus between sources and acceptors. RFD goes passively true indicating that all acceptors are "ready for data." A source will indicate the "data is valid" by pulling $\overline{DAV}$ low. Upon the reception of valid data by all acceptors, DAC will go passively true indicating that the "data has been accepted" by all acceptors.

Bus Management Lines ($\overline{ATN}$, $\overline{IFC}$, $\overline{SRQ}$, $\overline{EOI}$, $\overline{REN}$)—These lines are used to manage an orderly flow of information across the interface lines.

Attention ($\overline{ATN}$)—Is sent true over the interface to disable current talker and listeners freeing the signal lines ($\overline{IB0}$-$\overline{IB7}$). During the $\overline{ATN}$ active state devices monitor the DIO1 for addressing or an interface command. Data flows on the DIO1 lines when $\overline{ATN}$ is inactive (high).

Interface Clear ($\overline{IFC}$)—Is used to put the interface system into a known quiescent state.

Service Request ($\overline{SRQ}$)—Is used to indicate a need for attention in addition to requesting an interruption in the current sequence of events. This indicates to the controller that a device on the bus is in need of service.

Remote Enable ($\overline{REN}$)—is used to select one of two alternate sources of device programming data, local or remote control.

End of Identify ($\overline{EOI}$)—is used to signal the end of a multiple byte transfer sequence and in conjunction with $\overline{ATN}$ executes a parallel polling sequence.

Transmit/Receive Control Signals (T/$\overline{R}$ 1, T/$\overline{R}$ 2)—These two signals are used to control the quad transceivers which drive the interface bus. It is assumed that transceivers equivalent to the MC3448A will be used where each transceiver has a separate transmit/receive control pin. These pins can support one TTL load each. The outputs can then be grouped as shown in Figure 1 with $\overline{SRQ}$ hardwired high to transmit. The transmit/receive inputs of $\overline{REN}$, $\overline{IFC}$, and $\overline{ATN}$ are hardwired low to receive. $\overline{EOI}$ is controlled by T/$\overline{R}$1 through the MC3448A (or an equivalent) allowing it to transmit or receive. T/$\overline{R}$1 operates exactly as T/$\overline{R}$2 except during the parallel polling sequence. During parallel poll $\overline{EOI}$ will be made an input by T/$\overline{R}$1 while $\overline{DAV}$ and $\overline{IB0}$/$\overline{IB7}$ lines are outputs.

GPIA INTERNAL CONTROLS AND REGISTERS*

There are fifteen locations accessible to the MPU data bus which are used for transferring data to control the various functions on the chip and provide current chip status. Seven of these registers are write only and eight registers are read only. The various registers are accessed according to the three least significant bits of the MPU address bus and the status of the Read/Write line. One of the

*NOTE: Upper and lower case type designations will be used with the register bits to indicate remote or local messages respectively.

fifteen registers is external to the IC but an address switch register is provided for reading the address switches. Table 2 shows actual bit contents of each of the registers.

Data-In Register R7R—The data-in register is an actual eight-bit storage register used to move data from the interface bus when the chip is a listener. Reading the register does not destroy information in the data-out register. DAC (data accepted) will remain low until the MPU removes the byte from the data-in register. The chip will automatically finish the handshake by allowing DAC to go high. In RFD (ready for data) holdoff mode, a new handshake is not initiated until a command is sent allowing the chip to release holdoff. This will delay a talker until the available information has been processed.

DATA IN REGISTER
(Read Only)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

DI0-DI7 Correspond to DIO1-DIO8 of the 488-1975 Standard and IB0-IB7 of the MC68488

Data-Out Register R7W — The data-out register is an actual eight-bit storage register used to move data out of the chip onto the interface bus. Reading from the data-in register has no effect on the information in the data-out register. Writing to the data-out register has no effect on the information in the data-in register.

DATA OUT REGISTER
(Write Only)

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

DO0-DO7 Correspond to DIO1-DIO8 of the 488-1975 Standard and IB0-IB7 of the MC68488

Interrupt Mask Register R0W — The Interrupt Mask Register is a seven-bit storage register used to select the particular events that will cause an interrupt to be sent to the MPU. The seven control bits may be set independently of each other. If dsel (bit 7 of the Address Mode Register) is set high CMD bit 2 will interrupt on SPAS or RLC. If dsel is set low CMD will interrupt on UACG, UUCG, and DCAS in addition to RLC and SPAS. The Command Status

TABLE 2

	7	6	5	4	3	2	1	0	
R0W	IRQ	BO	GET		APT	CMD	END	BI	Interrupt "Mask" Reg.
R0R	INT	BO	GET		APT	CMD	END	BI	Interrupt Status Reg.
R1R	UACG	REM	LOK		RLC	SPAS	DCAS	UUCG	Command Status Reg.
R1W									Unused
R2R	ma	to	lo	ATN	TACS	LACS	LPAS	TPAS	Address Status Reg.
R2W	dsel	to	lo		hlde	hlda		apte	Address Mode Reg.
R3R	Reset	DAC	$\overline{DAV}$	RFD	msa	rtl	ulpa	fget	Auxiliary Command Reg.
R3W		rfdr	feoi	dacr			dacd		
R4R	UD3	UD2	UD1	AD5	AD4	AD3	AD2	AD1	Address Switch Reg.
R4W	lsbe	dal	dat	AD5	AD4	AD3	AD2	AD1	Address Register
R5R	S8	SRQS	S6	S5	S4	S3	S2	S1	Serial Poll Reg.
R5W		rsv1							
R6R	B7	B6	B5	B4	B3	B2	B1	B0	Command Pass-thru Reg.
R6W	PPR8	PPR7	PPR6	PPR5	PPR4	PPR3	PPR2	PPR1	Parallel Poll Reg.
R7R	D17	D16	D15	D14	D13	D12	DI1	DI0	Data In Register
R7W	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	Data Out Register

Register R1R may then be used to determine which command caused the interrupt. Setting GET bit 5 allows an interrupt to occur on Group Execute Trigger Command. END bit 1 allows an interrupt to occur if $\overline{EOI}$ is true (low) and $\overline{ATN}$ is false (high). APT bit 3 allows an interrupt to occur indicating that a secondary address is available to be examined by the MPU if apte (bit 0 of Address Mode Register) is enabled and listener or talker primary address is received and a Secondary Command Group is received. A typical response for a valid secondary address would be to set msa (bit 3 of Auxiliary Command Register) true and dacr (bit 4 Auxiliary Command Register) true, releasing the DAC handshake. BI indicates that a data byte is waiting in the data-in register. BI is set high when data-in register is full. BO indicates that a byte from the data-out register has been accepted. BO is set when the data-out register is empty. IRQ enabled high allows any interrupt to be passed to the MPU.

INTERRUPT MASK REGISTER

(Write Only)

IRQ	BO	GET	X	APT	CMD	END	BI

IRQ – Mask bit for IRQ pin
BO – Interrupt on byte output
GET – Interrupt on Group Execute Trigger
APT – Interrupt on Secondary Address Pass Through
CMD – Interrupt on SPAS + RLC + dsel (DCAS + UUCG + UACG) has occurred
END – Interrupt on EOI and ATN
BI – Interrupt on byte input

The Interrupt Status Register R0R — The Interrupt Status Register is a seven-bit storage register which corresponds to the interrupt mask register with an additional bit INT bit 7. Except for the INT bit the other bits in the status register are set regardless of the state of the interrupt mask register when the corresponding event occurs. The $\overline{IRQ}$ (MPU interrupt) is cleared when the MPU reads from the register. INT bit 7 is the logical OR of the other six bits ANDed with the respective bit of R0W.

INTERRUPT STATUS REGISTER

(Read Only)

INT	BO	GET	X	APT	CMD	END	BI

INT – Logical OR of all other bits in this register ANDed with the respective bits in the interrupt mask register.
BO – A byte of data has been output
GET – A Group Execute Trigger has occurred
APT – An Address Pass-Through has occurred
CMD – SPAS + RLC + dsel (DCAS + UUCG + UACG) has occurred
END – An EOI has occurred with $\overline{ATN}$ = 0
BI – A byte has been received

Serial Poll Register R5R/W — The Serial Poll Register is an eight-bit storage register which can be both written into and read by the MPU. It is used for establishing the status byte that the chip sends out when it is serial poll enabled. Status may be placed in bits 0 through 5 and bit 7. Bit 6 rsv (request for service) is used to drive the logic which controls the $\overline{SRQ}$ line on the bus telling the controller that service is needed. This same logic generated the signal SRQS which is substituted in bit 6 position when the status byte is read by the MPU $\overline{IB0}$–$\overline{IB7}$. In order to initiate a rsv (request for service), the MPU sets bit 6 true (generating rsv signal) and this in turn causes the chip to pull down the $\overline{SRQ}$ line. SRQS is the same as rsv when SPAS is false. Bit 6 as read by the MPU will be the SRQS (Service Request State).

SERIAL POLL REGISTER

(Read)

S8	SRQS	S6	S5	S4	S3	S2	S1

S1-S8 – Status bits
SRQS – Bus in Service Request State

SERIAL POLL REGISTER

(Write)

S8	rsv	S6	S5	S4	S3	S2	S1

S1-S8 – Status bits
rsv – generate a service request

Parallel Poll Register R6W — This register may be loaded by the MPU and the bits in this register will be delivered to the instrument bus IB0–IB7 during PPAS (Parallel Poll Active State). This register powers up in the PP0 (Parallel Poll No Capability) state. The reset bit (Auxiliary Command Register bit 7) will clear this register to the PP0 state.

The parallel poll interface function is executed by this chip using the PP2 subset (Omit Controller Configuration Capability). The controller cannot directly configure the parallel poll output of this chip. This must be done by the MPU. The controller will be able to indirectly configure the parallel poll by issuing an addressed command which has been defined in the MPU software.

PARALLEL POLL REGISTER

(Write Only)

PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1

Bits delivered to bus during Parallel-Poll Active State (PPAS)
Register powers up in the PP0 state
Parallel Poll is executed using the PP2 subset

Address Mode Register R2W — The address mode register is a storage register with six bits for control: to, lo, hide, hlda, dsel, and apte. The to bit 6 selects the talker/listener and addresses the chip to talk only. The lo bit 5 selects the talker/listener and sets the chip to listen only. The apte bit 0 is used to enable the extended addressing mode. If apte is set low the device goes from the TPAS (Talker Primary

Address State) directly to the TADS (Talker Addressed State). The hlda bit 2 holds off RFD (Ready for Data) on ALL DATA until rfdr is set true. The hlde bit 3 holds off RFD on EOI enabled (low) and ATN not enabled (high). This allows the last byte in a block of data to be continually read as needed. Writing rfdr true (high) will allow the next handshake to proceed.

ADDRESS MODE REGISTER

(Write Only)

dsel	to	lo	X	hdle	hdla	X	apte

dsel – configure for automatic completion of handshake sequence on occurrence of GET, UACG, UUCG, SDC, or DCL commands
to – set to talk-only mode
lo – set to listen-only mode
hdle – Hold-off RFD on end
hdla – Hold-off RFD on all data
apte – Enable the address pass-through feature

Address Status Register R2R — The address status register is not a storage register but simply an eight-bit port used to couple internal signal nodes to the MPU bus. The status flags represented here are stored internally in the logic of the chip. These status bits indicate the addressed state of the talker/listener as well as flags that specify whether the chip is in the talk only or listen only mode. The ATN, bit 4, contains the condition of the Attention Line. The ma signal is true when the chip is in:

TACS — Talker Active State
TADS — Talker Addressed State
LACS — Listener Active State
LADS — Listener Addressed State
SPAS — Serial Poll Active State

ADDRESS STATUS REGISTER

(Read Only)

ma	to	lo	ATN	TACS	LACS	LPAS	TPAS

ma – my address has occurred
to – the talk-only mode is enabled
lo – the listen-only mode is enabled
ATN – The Attention command is asserted
TACS – GPIA is in the Talker Active State
LACS – GPIA is in the Listener Active State
LPAS – GPIA is in the Listener Primary Addressed State
TPAS – GPIA is in the Talker Primary Addressed State

Address Switch Register R4R — The address switch register is external to the chip. There is an enable line ($\overline{ASE}$) to be used to enable three-state drivers connected between the address switches and the MPU. When the MPU addresses the address switch register the enable line directs the switch information to be sent to the MPU. The five least significant bits of the eight-bit register are used to specify the bus address of the device and the remaining three bits may be used at the discretion of the user. The most probable use of one or two of the bits is for controlling the listener only or talk only functions.

ADDRESS SWITCH REGISTER

(Read Only)

UD3	UD2	UD1	AD5	AD4	AD3	AD2	AD1

AD1–AD5 – Device address
UD1–UD3 – User definable bits
When this "register" is addressed, the $\overline{ASE}$ pin is set which allows external address switch information from bus device to be read.

Address Register R4W — The Address Register is an eight-bit storage register. The purpose of this register is to carry the primary address of the device. The primary address is placed in the five least significant bits of the register. If external switches are used for device addressing these are normally read from the Address Switch Register and then placed in the Address Register by the MPU.

AD1 through AD5 bits 0–5 are for the device's address. The lsbe bit 7 is set to enable the Dual Primary Addressing Mode. During this mode the device will respond to two consecutive addresses, one address with AD1 equal to 0 and the other address with AD1 equal to 1. For example, if the device's address is HEX 0F, the Dual Primary Addressing Mode would allow the device to be addressed at both HEX OF and HEX OE. The dal bit 5 is set to disable the listener and the dat bit 5 is set to disable the talker.

This register is cleared by the $\overline{Reset}$ input only (not by the reset bit of the Auxiliary Command Register bit 7).

When $\overline{ATN}$ is enabled and the primary address is received on the $\overline{IB0-7}$ lines, the MC68488 will set bit 7 of the address status register (ma). This places the MC68488 in the TPAS or LPAS.

When $\overline{ATN}$ is disabled the GPIA may go to one of three states: TACS, LACS or SPAS.

ADDRESS REGISTER

(Write Only)

lsbe	dal	dat	AD5	AD4	AD3	AD2	AD1

lsbe – enable dual primary addressing mode
dal – disable the listener
dat – disable the talker
AD1-AD5 – Primary device address, usually read from address switch register
Register is cleared by the $\overline{Reset}$ input pin only.

Auxiliary Command Register R3R/W — Bit 7, reset, initializes the chip to the following states: (reset is set true by external $\overline{Reset}$ input pin and by writing into the register from the MPU).

SIDS—Source Idle State
AIDS—Acceptor Idle State
TIDS—Talker Idle State
LIDS—Listener Idle State

LOCS—Local State
NPRS—Negative Poll Response State
PPIS—Parallel Poll Idle State
PUCS—Parallel Poll Unaddressed to Configure State
PPO—Parallel Poll No Capability

rfdr (release RFD handshake) bit 6 allows for completion of the handshake that was stopped by RFD (Ready For Data) holdoff commands hlda and hlde.

fget (force group execute trigger) bit 0 has the same effect as the GET (Group Execute Trigger) command from the controller.

rtl (return to local) bit 2 allows the device to respond to local controls and the associated device functions are operative.

dacr (release DAC handshake) bit 4 is set high to allow DAC to go passively true. This bit is set to indicate that the MPU has examined a secondary address or an undefined command.

ulpa (upper/lower primary address) bit 1 will indicate the state of the LSB of the address received on the DIO1-8 bus lines at the time the last Primary Address was received. This bit can be read but not written by the MPU.

msa (valid secondary address) bit 3 is set true (high) when TPAS (Talker Primary Addressed State) or LPAS (Listener Primary Addressed State) is true. The chip will become addressed to listen or talk. The primary address must have been previously received.

RFD, $\overline{DAV}$, DAC—(Ready For Data, Data Valid, Data Accepted) bits assume the same state as the corresponding signal on the MC68488 package pins. The MPU may only read these bits. These signals are not synchronized with the MPU clock.

dacd (data acceptdisable) bit 1 set high by the MPU will prevent completion of the automatic handshake on Addresses or Commands. dacr is used to complete the handshake.

feoi (forced end or identify) bit 5 tells the chip to send $\overline{EOI}$ low. The $\overline{EOI}$ line is then returned high after the next byte is transmitted. NOTE: The following signals are not stored but revert to a false (low) level one clock cycle (MPUϕ2) after they are set true (high):

1. rfdr
2. feoi
3. dacr

These signals can be written but not read by the MPU.

AUXILIARY COMMAND REGISTER

reset	rfdr	feoi	dacr	msa	rtl	dacd	fget	Write
	DAC	$\overline{DAV}$	RFE			ulpa		Read

reset — initialize the chip to the following status;
(1) all interrupts cleared
(2) following bus states are in effect: SIDS, AIDS, TIDS, LIDS, LOCS, PPIS, PUCS, and PPØ
(3) bit is set by $\overline{Reset}$ input pin
msa — if GPIA is in LPAS or TDAS, setting msa will force GPIA to LADS or TADS
rtl — return to local if local lockout is disabled
ulpa — state of LSB of bus at last-primary-address receive time
fget — Force group execute trigger command from the MPU has occurred
rfdr — continue handshake stopped by RFD holdoff
feoi — set EOI true, clears after next byte transmitted
dacr — MPU has examined an undefined command or secondary address
dacd — prevents completion of automatic handshake on Addresses or Commands

Command Status Register R1R — The command status register flags commands or states as they occur. These flags or states are simply coupled onto the MPU bus. There are five major address commands REM shows the remote/local state of the talker/listener. RLC bit 3 is set when a change of state of the remote/local flip-flop occurs and reset when the command status register is read. DCAS bit 1 indicates that either the device clear or selected device clear has been received activating the device clear function. SPAS bit 2 indicates that the SPE command has been received activating the device serial poll function. UACG bit 7 indicates that an undefined address command has been received and depending on programming the MPU decides whether to execute or ignore it. UUCG bit 0 indicates that an undefined universal command has been received.

COMMAND STATUS REGISTER
(Read)

UACG	REM	LOK	X	RLC	SPAS	DCAS	UUCG

UACG — Undefined Addressed Command
REM — Remote Enabled
LOK — Local Lockout Enabled
RLC — Remote/Local State Changed
SPAS — Serial Poll Active State is in effect
DCAS — Device Clear Active State is in effect
UUCG — Undefined Universal Command

Command Pass-Through Register R6R — The command pass through is an eight-bit port with no storage. When this port is addressed by MPU it

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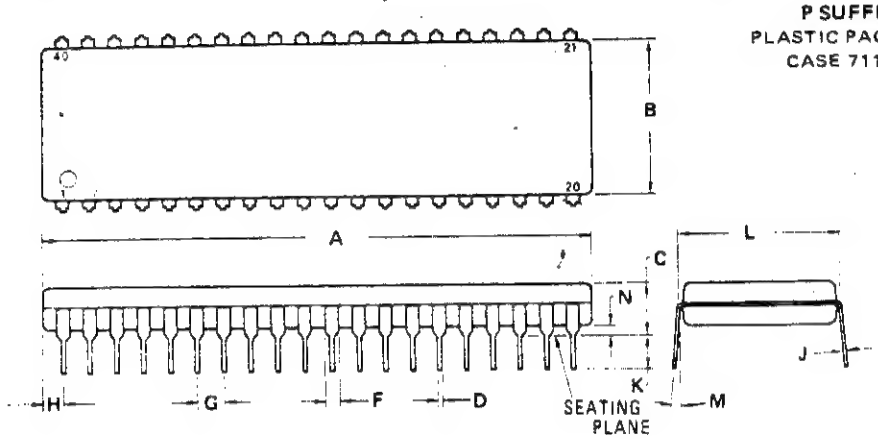
connects the instrument data bus ($\overline{IB0}$–$\overline{IB7}$) to the MPU data bus D0–D7. This port can be used to pass commands and secondary addresses that aren't automatically interpreted through to the MPU for inspection.

COMMAND PASS-THROUGH REGISTER

(Read Only)

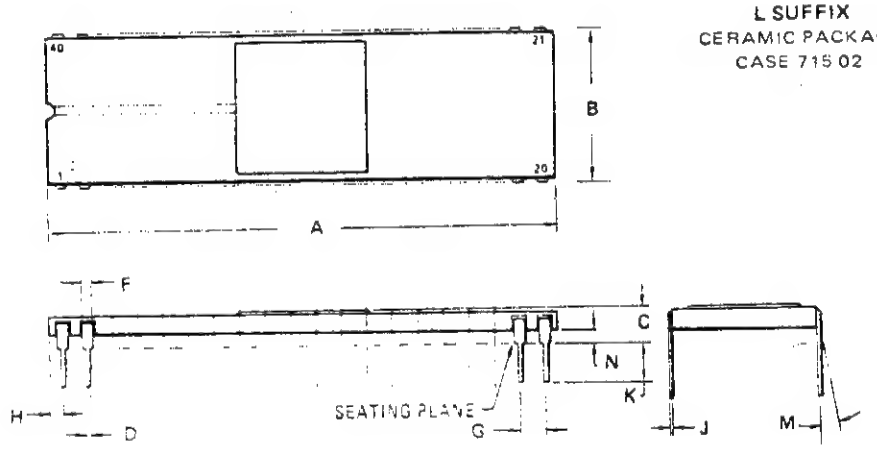
B7	B6	B5	B4	B3	B2	B1	BØ

An eight-bit input port used to pass commands and secondary addresses to MPU which are not automatically interpreted by the GPIA



P SUFFIX
PLASTIC PACKAGE
CASE 711-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.68	4.19	0.145	0.165
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040



L SUFFIX
CERAMIC PACKAGE
CASE 715-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.

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